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Original Research Article

Cat Swarm Intelligence-Driven Optimization for High Power Factor Single-Stage AC–DC Converters

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Abstract: A line-coupled single-stage AC–DC converter is introduced to adjust both the output voltage and the DC link voltage, ensuring optimal power factor correction (PFC) during boost and PFC operating modes. In this approach, the control strategy minimizes the error signal and generates appropriate switching pulses for the converter by integrating the Cat Swarm Optimization (CSO) algorithm with a Fractional Order PID (FOPID) controller. The CSO algorithm determines the optimal control pulses to diminish the error in the PFC process, and its output is subsequently applied as input to the FOPID controller. This enables the precise tuning of gain parameters, thereby improving the dynamic response and stability of the controller. By adopting this optimal switching strategy, the complexity associated with error voltage variation is effectively minimized. The proposed system is demonstrated and simulated in the MATLAB/Simulink environment, and its performance is analyzed. Finally, the outcomes are related against existing optimization methods such as Firefly Algorithm (FA) and Cuckoo Search (CS), demonstrating the superiority of the proposed technique.

Keywords - Cat Swarm Optimization (CSO) algorithm, Power Factor Correction (PFC), Fractional Order proportional integral derivative (FOPID), AC to DC converter, Firefly Algorithm (FA) and Cuckoo Search (CS) algorithm.

INTRODUCTION

These days, the uses of AC/DC switch-mode converters, for example, PC control supplies, battery chargers, and other electronic gear, are quickly developing and result in some power quality issues [1, 2]. This hardware comprises of semiconductor gadgets that indicate nonlinear conduct and work at high frequencies [3]. Consequently, these gadgets infuse numerous consonant unsettling influences into the system and lessen the power factor [4]. Lately, new directions have encouraged enthusiasm for Power Factor Correction (PFC) systems for lessen the unsettling influence in the system [5, 6]. The interest for PFC has been expanding for the present disconnected power supplies and even those at low power levels. The disconnected AC-DC device converters utilized in a large portion of the present electrical gear have been a noteworthy wellspring of consonant bending drawing mutilated flow waveforms, dirtying the mains, and accordingly corrupting force quality [7, 8]. Today, a made converter ought to fulfill satisfactory power quality measurements. Power quality issues have dependably

been a critical theme in power designing, be that as it might, as of late, this point has drawn an uncommon consideration because of the expanded utilization of elite electronic gadgets [9, 10].

With the rising mandate for high-quality power factor systems, power factor improvement has develop a critical aspect in converter design [11]. To address this, both single-stage and two-stage converter topologies are widely adopted. The two-stage configuration offers high power factor and fast output voltage response by employing independent controllers and separate power stages [12, 13]. Nevertheless, the approach suffers from certain key drawbacks the increased cost and bulkiness arising from the complex circuit structure, making it less suitable for low-power applications [14]. To address these boundaries, single-stage clarification systems have been developed that integrate the PFC phase and the DC/DC converter into a unified structure. Typically, these single-stage PFC converters employ a boost topology operating in Discontinuous Conduction Mode to realize effective power factor correction [15]. DCM operation generally results in lower Total Harmonic Distortion (THD) of the input current compared to Continuous Conduction Mode (CCM), although CCM provides slightly higher efficiency than DCM[15].

AC–DC converters performance an energetic part in power electronic systems due to their advantages of low cost and ease of implementation [16]. Simultaneously, they lead to multiple operational challenges that can unfavorably impression the system, such as feeder overloading, harmonic distortion, high investment cost, reduced efficiency, and limited reliability, which hinder their extensive adoption [17, 18]. The overall size and cost of a converter largely depend on its regulator strategy, which should ideally be optimized for the best performance. Operating at higher switching frequencies, however, increases transistor switching losses, thereby limiting efficiency. To enhance control and power factor correction (PFC), Frequent performances have been scrutinized in prior research , including Artificial Neural Networks (ANN), Control Lyapunov functions, discrete energy functions, Fuzzy Logic Controllers (FLC) [19], Adaptive Neuro-Fuzzy Inference Systems (ANFIS), Particle Swarm Optimization (PSO), and Genetic Algorithms (GA) [20]. Nevertheless, these methods often struggle to deliver best presentation under fluctuating load circumstances, which leads to degradation in the overall power superiority of the organization and necessitates more effective solutions. In this work, a Cat Swarm Optimization (CSO) constructed control technique integrated with a Fractional Order PID (FOPID) controller is anticipated for achieving optimal PFC in an AC–DC converter. The method regulates the DC association voltage by comparing the actual load voltage with a reference voltage, where the variation over time is processed through the CSO–FOPID framework. Based on these variations, the appropriate switching mode is determined to maintain efficient operation. The usefulness of the anticipated approach is authenticated by comparing the output voltage presentation of the AC–DC converter against existing FA and CS algorithms. The paper is organized as follows: Section 2 discusses related work; Section 3 outlines the proposed methodology and PFC stage operation; Section 4 reports the implementation and simulation results; and Section 5 summarizes the conclusions.

LITERATURE REVIEW

Quantities of research work are exhibited to break down the Power factor improvement of the AC-DC converters. A portion of the works is reconsidered here.

According to Nor Azura Samsudin *et al.* [21], a single-phase AC/DC converter incorporating PFC and a hybrid full-bridge rectifier was designed and experimentally analyzed for LED streetlight applications. The converter utilized one LLC resonant tank, two boost circuits, and a shared inductor. By employing a transfer switch at the secondary side, the converter could function as either a conventional full-bridge rectifier or a full-bridge voltage-doubler rectifier. Hongfei Wu *et al.* [22] proposed quasi–single-stage AC–DC power converters based on a three-port bridgeless PFC topology. The three-port bridgeless PFC (TPB-PFC) was designed to simultaneously deliver an AC input port, a DC load port, and a DC bus port by incorporating an additional DC load port into a conventional bridgeless PFC structure. Abderrahmen Benyamina *et al*. [23] have suggested a plan and a constant utilization of a ANFIS based voltage controller for a solitary stage support solidarity Active Power Factor Correction (APFC) so as to enhance its exhibitions. The control enhances the DC transport voltage circle and displayed a decent ability to follow the voltage reference point under a quick variety of the heap with less vacillation in the consistent state. Muntasir Alam et al. [24] proposed a Hybrid Resonant Pulse-Width Modulation (HRPWM) bridgeless air-conditioning DC power factor correction (PFC) boost converter for use in power supplies and battery charging applications.

In bridgeless mode, the converter operates without a front-end diode bridge rectifier, thereby reducing transference losses. Because the PWM switches are controlled using a common gating signal, the circuit eliminates the need for extra hardware to differentiate amongst the positive and negative half-cycles of the alternate current input. This simplification lowers hardware complexity, minimizes power loss, and progresses the overall efficiency of the converter [33].

Mohamed O. Badawy et al. [25] proposed a dual-switch controlled configuration for an AC/DC non-inverting buck-boost PFC converter. The converter operates in a variable capacitor voltage mode, achieving an inherently high power factor along with zero-voltage switching. Additionally, the control scheme ensures a distortion-free sinusoidal input current across a wide range of output voltage levels. Unlike conventional methods, this approach eliminates the need for a mode detector, thereby avoiding abrupt transitions between buck and boost operations. Although both switches are utilized, only a single feedback control loop is sufficient to regulate the desired power flow at unity power factor. The proposed system employs a Cat Swarm Optimization (CSO) algorithm with a Fractional Order PID (FOPID) controller for efficient power factor regulation in a single-phase AC–DC converter, and the detailed control process is discussed in the subsequent section.

Organization of the Planned Method

This subdivision offerings the design and description of the PFC strategy for a line-coupled single-stage AC–DC converter. In this approach, an optimal control mechanism is developed specifically for single-stage operation, where The proposed topology integrates both power factor correction (PFC) and DC–DC voltage regulation functionalities into a single-stage configuration. The primary objective of the proposed control system is twofold: to achieve input power factor correction and to regulate the DC-link voltage at the output. To accomplish this, a line-coupled single-stage AC–DC converter is designed, and a novel control strategy is subsequently developed to enhance system performance. The integration of the designed converter with the proposed control scheme results in the realization of an optimal controller for enhanced performance.

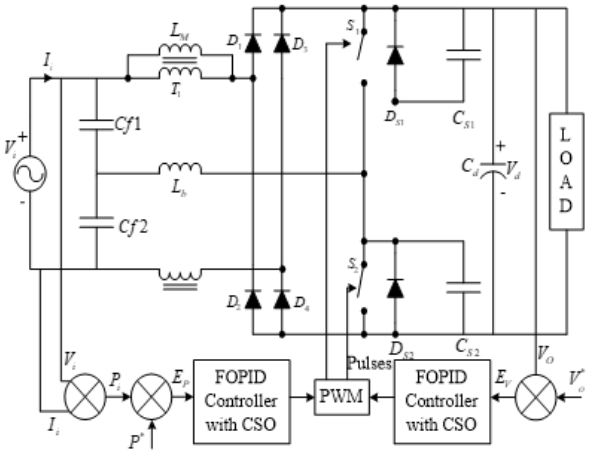


Fig.1 Structure of proposed single-stage line-coupled AC to DC converter

A single-stage line-coupled AC–DC Converter with enhanced power factor capability and ripple-free input current is proposed, as illustrated in Figure 1. In this configuration, the PFC stage and the DC–DC conversion stage are integrated by sharing two active switches, thereby reducing circuit complexity. The practice of a together inductor enables the planned converter to achieve near-unity power factor while ensuring a smooth, ripple-free input current. The switching devices operate with complementary duty cycles, which are modulated to normalize the output voltage. Under AC input conditions, the main inductor and associated circuit elements maintain continuous current flow during switching transitions. In this work, the converter's input control is regulated to accurately track a predefined reference profile, ensuring that the input current remains in phase with the input voltage and thereby achieving effective power factor correction. This redresses the power factor of information control supply. Here the count of blunder esteem is given as,

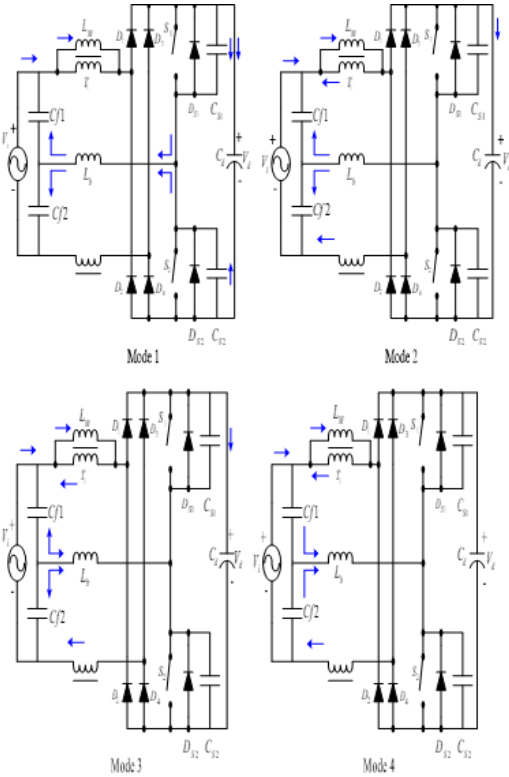
$$EV = P^{*}(t) - P_i(t) \quad (1)$$

$$P_i(t) = V_i(t) - I_i(t) \quad (2)$$

Equation (2) defines the actual input power distributed to the converter. The proposed control approach adjusts the input current based on this power value, ensuring that it remains directly proportionate to the input voltage which is considered constant throughout the converter's operation. Consequently, power factor improvement is achieved by aligning the input current waveform with the input voltage waveform. In simpler terms, the input power is regulated to follow its reference value. The resulting error, calculated from equation (1), is then used to generate the control signal for the PWM modulator, which in turn produces the gating pulses required to drive the power switches.

Operation of PFC stage

The future PFC circuit operating modes are illustrated, i_{Cf1} and i_{Cf2} the flows coursing through the channel capacitors $Cf1$ and $Cf2(Cf1=Cf2=Cf)$ separately. i_{Lb} is the present finishing the inductor L_b . As can be demonstrates the coupled inductor is displayed as the charging inductance L_{m1} and perfect transformer which has a turn proportion of 1:1 [26]. The L_{m1} is the charging inductance has been sufficiently vast to keep up a steady current i_{m1} inside a switching period.



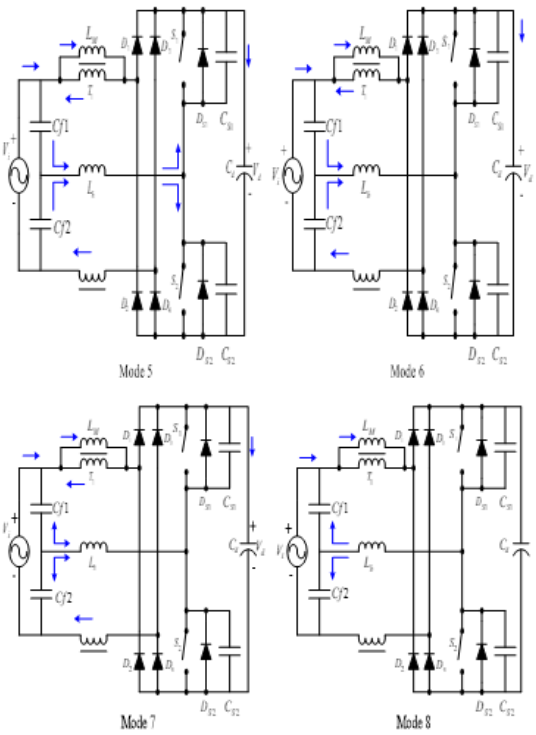


Fig.2 Operating modes of the PFC stage

The consistent state task of the PFC circuit in one swapping period T_S incorporates eight modes, as shows in Figure 2. Switches S_1 and S_2 are worked lopsidedly and the duty ratio D depends on the switch S_2 . The activity displays symmetry for the two scopes of the responsibility ratio D from 0 to 0.5 and from 0.5 to 1. Without loss of simplification, the converter is measured with the duty ratio D from 0 to 0.5. To represent the relentless state task, it is expected that all segments are perfect [27]. The swell part of the dc-link voltage V_d is irrelevant on the grounds that the dc-link capacitor C_d has a vast esteem. It is expected that the supply voltage V_i is viewed as littler than the dc-link voltage V_d and steady for an exchanging period. At that point the capacitor current $Cf1$ moves toward becoming,

$$i_{Cf1} = Cf1.\left(\frac{dV_{Cf1}}{dt}\right) = Cf1.\left(\frac{d\left(V_i - V_{Cf2}\right)}{dt}\right) = -Cf1\left(\frac{dV_{Cf2}}{dt}\right) = -i_{Cf2} \quad (3)$$

Since $i_{Cf1} = i_{Cf2} + i_{L_b}$, $i_{Cf1} = 0.5 i_{L_b}$. Along these lines, a similar measure of current courses through every one of the capacitors. At the point when $Cf1$ is charging, $Cf2$ is discharging. Conversely when $Cf2$ is charging, $Cf1$ is discharging. In this charge exchange, the swell part of the channel capacitor voltages V_{Cf1} and V_{Cf2} is immaterial on the grounds that the channel capacitors $Cf1$ and $Cf2$ have extensive qualities. Subsequently V_{Cf1} and V_{Cf2} are viewed as steady. Before Mode 1, the lift inductor current i_{L_b} streams with the peak value $-I_{L_b}$ through and D_1, S_1 and L_b .

Operation of mode 1:

The upper switch S_1 is turned off. Then, the inductor current i_{L_b} starts to charge C_{S1} and C_{S2} discharge. The voltage V_{S1} across the upper switch S_1 increases and the voltage across the lower switch S_2 decreases. Since the switch capacitors C_{S1} and $C_{S1} = C_{S1} = C_S$ associated in parallel with the switches and have a small value. Therefore, the inductor current i_{L_h} has constant value.

Operation of mode 2:

The voltage V_{S2}, through the lower switch S_2 develops zero. Then, the lower diode D_{S2} and the diode D_4 are turned on. Since $V_{Cf1} = -V_{L_b} + V_T + V_d$ and $V_{Cf2} = V_{L_b} + V_T$, the voltage V_T across the coupled inductor T_1 and the voltage L_b across the inductor are given by,

$$V_T(t) = -\frac{V_d - V_i}{2} \quad (4)$$

$$V_{L_b}(t) = V_{Cf2} - V_T \quad (5)$$

Operation of mode 3:

The lower switch S_2 is turned on. Zero voltage turn on of S_2 is achieved because the current has previously flown through the lower diode D_{S_2} before the lower switch S_2 is turned on. S_2 has only to be turned on before variations its direction. The inductor current i_{L_b} and the current i_2 increase linearly like mode 2. The inductor current i_{L_b} and the current i_2 approach I_{L_b} to at the end of mode 3.

When the lower switch S_2 is turned ON, zero-voltage switching is achieved since the current is already flowing through the corresponding lower diode prior to the switching action. Thus, S_2 only needs to be turned ON before the current variations its direction. During this interval, the inductor current S_2 and the load current S_2 increase linearly, similar to the behavior observed in Mode 2. By the end of Mode 3, both the inductor current and the load current gradually approach the reference value S_2.

Operation of mode 4:

The primary current i_1' of the ideal transformer arrives at $-I_{L_b}$ and the diode D is turned off. Since the current i_1' is clamped at $-I_{L_b}$, the current i_2 and the current i_{L_b} are also clamped at I_{L_b}. The voltage V_T is fixed to V_{Cf2}.

Operation of mode 5:

The lower switch S_2 is turned off. Then, the inductor current i_{L_b} starts to discharge C_{S1} and C_{S2} charge. The upper switch voltage V_{S1} decreases and the lower switch voltage V_{S2} increases.

Operation of mode 6:

The voltage V_{S1} across the upper switch S_1 becomes zero. Then, the diode D_{S1} and the diode D_1 are turned on. Since $V_{Cf1} = -V_{L_b} + V_T$ and $V_{Cf2} = V_{L_b} + V_T + V_d$, the voltage V_T and the voltage V_{L_b} are given by,

$$V_T(t) = -\frac{V_d - V_i}{2} \quad (6)$$

$$V_{L_b}(t) = -(V_{Cf1} - V_T) \quad (7)$$

Operation of mode 7:

The upper switch S_1 is turned on. Zero voltage turn on of the upper switch is achieved similarly in mode 3. The inductor current i_{L_b} and the current i_2 decrease linearly like mode 6. The current i_{L_b} and the current i_2 approach to $-I_{L_b}$ and zero respectively, at the end of mode 7.

Operation of mode 8:

The current i_2 arrives at zero and the diode D_4 is turned off. Since the inductor current is i_{L_b} clamped at $-I_{L_b}$, the voltage across the inductor L_b is zero and the voltage V_T is fixed to V_{Cf1}. Then the error value has been minimization of using FOPID controller, which is tuning the gain parameters. The FOPID supervisor has been achieved the reduced the error value and controlling PWM. The detailed process of FOPID controller has been give below,

3.2. Description of FOPID controller

The Fractional Order Proportional-Integral-Derivative controller is an advanced extension of the classical PID controller, achieved by applying fractional-order calculus to the integral and derivative components. This generalization offers several performance benefits, such as the complete elimination of steady-state error, enhanced flexibility in tuning gain and phase crossover frequencies, and improved stability margins. In accumulation, the FOPID supervisor demonstrates strong robustness against variations in system dynamics and ensures better attenuation of high-frequency noise. These attributes make it a controlling mechanism strategy for handling complex, nonlinear, and uncertain systems [28].

Numerically the FOPID controller can be defined as equation (8),

$$u(t) = K_P EV(t) + K_I \int_0^t EV(t)dt + K_D \frac{dEV(t)}{dt} \quad (8)$$

On performing the Laplace transform of the equation (9),

$$L_F(s) = K_p + \frac{K_i}{t^{\lambda}} + K_d s^{\mu} \quad (9)$$

Where, K_p signifies the gain of proportionality, K_i signifies the gain of Integral, K_d signifies the gain of Derivative and λ and μ are the differential-integral's order for FOPID controller as demonstrated in figure 3 (i) where λ and μ can be any real numbers.

The traditional PID controller can be considered a specific case of the Fractional Order PID controller, obtained by fixing the fractional integral and derivative orders to unity [29]. This demonstrates that the FOPID controller broadens the capabilities of the classical PID by introducing additional notches of autonomy in tuning. As a result, it provides improved flexibility in adjusting system dynamics, thereby enhancing both the reliability and the overall recital of the control system.In addition, the FOPID controller increases system robustness against sudden disturbances, contributing to improved stability. However, unlike the PID controller which requires tuning of three parameters, the FOPID controller involves five parameters, making the design process more challenging. The primary objective of tuning these parameters is to minimize the performance index, thereby improving the stability margin of the hybrid system.

This approach improves the damping characteristics of the organization and minimizes deviations in terminal voltage, thereby reducing the error among input and output power. To evaluate controller performance, standard presentation indices such as the Integral of Absolute Error (IAE), Integral of Squared Error (ISE), and Integral of Squared Time Error (ISTE) are employed. These indices, expressed in equations (10), (11), and (12), serve as key measures for assessing system accuracy and stability.

$$IAE = \int_0^{\infty} |EV(t)| dt \quad (10)$$

$$ISE = \int_0^{\infty} EV(t)^2 dt \quad (11)$$

$$ISTE = \int_0^{\infty} tEV(t)^2 dt \quad (12)$$

It is always required to select a reference model to get the error function $EV(t)$. The smaller the error function, the closer the controlled system response is to the reference model. In this context, the performance of the FOPID controller can be evaluated using equations (13) and (14).

$$J(K_P, K_I, K_D, \lambda, \mu) = \int_0^{\infty} |V_o^*(t) - V_o(t)| dt \quad (13)$$

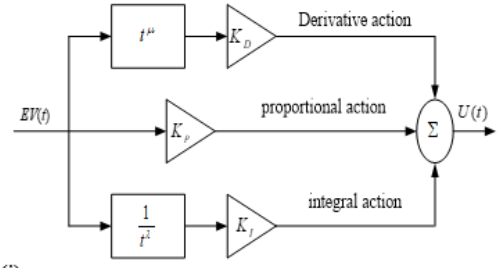
$$J(K_P, K_I, K_D, \lambda, \mu) = \int_0^{\infty} \left| P^*(t) - P_i(t) \right| dt \quad (14)$$

Here, $V_o^*(t)$ is the reference output voltage, $V_o(t)$ is the output voltage, $P^*(t)$ is the reference power and $P_i(t)$ is the input power of the system.

The regulation of FOPID supervisor parameters is accomplished by minimizing an appropriate objective function, where the assortment of the fitness role plays a critical role in determining the usefulness of the optimization. Performance indices such as the Integral of Absolute Error (IAE) and the Integral of Squared Error (ISE) are commonly used to evaluate the dynamic performance and accuracy of control systems., though they often result in longer settling times despite providing low overshoot. To overcome this limitation, the Integral of Squared Time multiplied by Error criterion is sometimes employed, as it enhances transient response; however, it also increases computational complexity and does not always guarantee desired stability. In this work, the FOPID controller parameters are adjusted online using the Cat Swarm Optimization algorithm, which directly regulates the DC-link voltage, generates the PWM control signals, and minimizes the error for the AC–DC converter.

Process of the CSO algorithm for optimization of dc link voltage

A novel meta-heuristic optimization technique inspired by the color-changing behavior of cats is utilized to achieve optimal power factor correction (PFC) in a line-coupled single-stage AC–DC converter, wherein the Cat Swarm Optimization (CSO) algorithm is specifically employed to optimize the DC-link voltage for enhanced performance and efficiency. The controller gain parameters are initially generated randomly, while system variables such as power and voltage are taken as inputs to the algorithm. The primary objective function is defined to minimize both the error value and the DC-link voltage deviation. Once the optimization process is complete, the corresponding gain parameters are obtained and organized into a dataset for further controller design and performance evaluation.In the CSO algorithm process, the improvement and error values are trained and achieve the best results for the FOPID controllers.



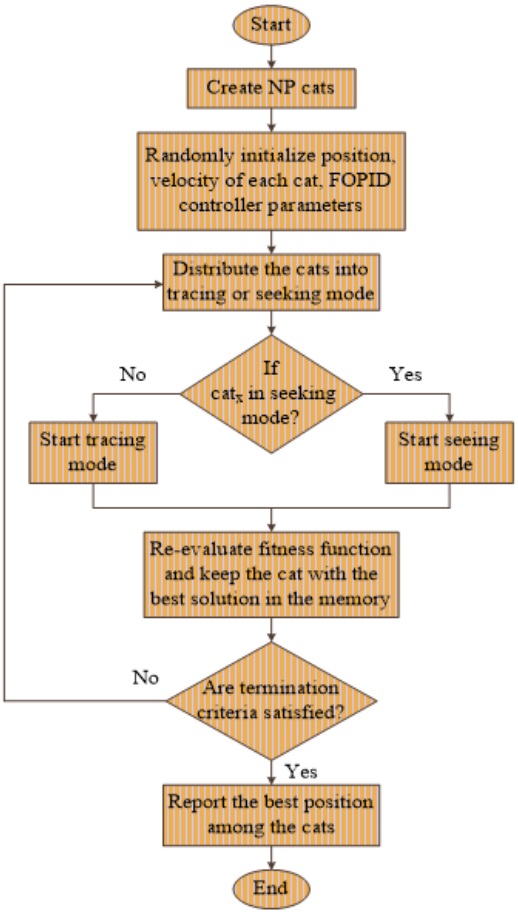


Fig.3 The Flow diagram of (i) FOPID controller and (ii) proposed method

Established on the controller's output, transformation algorithms are applied to generate the optimal switching pulses for the AC–DC converter.

This section explains the basic working principle of the Cat Swarm Optimization algorithm. The CSO approach is derived from the behavioral patterns of cats [30], which generally devote much of their time to resting and monitoring their environment, conserving energy by limiting unnecessary movements. This characteristic is mathematically represented in the algorithm through two operating modes: the seeking mode, which corresponds to the cat's alert and observant resting state used for exploration of possible solutions, and the tracing mode, which mimics the cat's chasing action used for exploitation of promising solutions.

***Seeking mode:* Resting and Observing:**
In the CSO algorithm, the seeking mode simulates the behavior of cats during their sleeping state, where they remain vigilant and observe their environment to decide on the next move [31]. This mode is characterized by four essential parameters: the Seeking Memory Pool , which stores possible candidate solutions; the Seeking Range of the Selected Dimension, which specifies the extent of parameter variation; the Count of Dimensions to Change , which determines the number of variables adjusted during the search; and the Self-Position Consideration , which defines whether the cat's current position should be retained as a candidate solution. Collectively, these parameters allow effective exploration of the solution space.

Tracing Mode – Pursuing a Target:
The tracing mode represents the active hunting behavior of cats. In this phase, a cat updates its position by adjusting its velocity in each dimension, thereby moving towards the target solution. This mode emphasizes exploitation, enabling the algorithm to refine promising areas of the search space for optimal results.

CSO movement= Seeking mode + Tracing mode
When relating the CSO algorithm to resolve optimization problems, the preliminary step is to type a resolution on the number of individuals or cats to use. Each cat in the population has the following characteristics [32].

* Each cat's position is defined in an M-dimensional search space.
* Every dimension of the position is associated with a corresponding velocity.
* The fitness of a cat is evaluated based on a predefined fitness function.
* A mode flag is assigned to indicate whether the cat is operating in seeking mode or tracing mode.

Steps of the CSO algorithm:

Step 1: Initially, the FOPID supervisor parameters are initiated randomly such as, K_P, K_I, K_D, λ and μ respectively. The primary parameters of CSO algorithm create the number of population (ψ) with randomly initialize position, velocity within respective boundaries for each cat.

Step 2: Based on the value of the Mixture Ratio (MR), each cat is assigned a specific flag to categorize it into either the seeking mode or the tracing mode process.

Step 3: Evaluate the fitness value of each cat and record the one with the highest fitness as the best-performing solution.

Step 4: Cats are updated according to their assigned flags—those in seeking mode undergo the seeking process, while the others follow the tracing process. The position of each cat in a given dimension is then updated using equation (15).

$$V_{x,d} = V_{x,d} + R_1.C_1.\left(A_{best,d} - A_{x,d}\right), \quad d = 1,2,....., M \tag{15}$$

Where, $V_{x,d}$ is the velocity of cat x in dimension d, $A_{best,d}$ is the position of the cat, who has the best fitness value, $A_{x,d}$ is the position of cat_x, C_1 is a constant and R_1 is A random value within the range [0, 1] is generated to determine the cat's velocity, enabling it to move through the M-dimensional decision space and record each new position. If the computed velocity exceeds the maximum allowable limit, it is adjusted to the maximum value, after which the new position of each cat is calculated accordingly.

$$A_{x,d,new} = A_{x,d,old} + V_{x,d} \tag{16}$$

Where, $A_{x,d,new}$ is the new position of cat x in dimension d and $A_{x,d,old}$ is the current position of cat x in dimension d respectively.

Step 5: Select a new subset of cats based on the mixture ratio (MR) and assign them to the tracing mode, while the remaining cats are allocated to the seeking mode.

Step 6: The algorithm then evaluates the termination condition. If the condition is met, the optimization process concludes; otherwise, the procedure iteratively continues by repeating Steps 3 through 5.

The CSO algorithm is optimized automatically by seeking mode and tracing mode operation. Because of its flexibility, the CSO algorithm can be used for a wide range of control applications. The Figure 3 (ii) describes the optimization flow of the CSO algorithm for minimize the error values and PFC in the AC to DC converter. The proposed algorithm is implemented in the subsequent section to design an FOPID controller for optimizing the power factor correction (PFC) in a line-coupled single-stage AC–DC converter system. In this control framework, the FOPID controller is trained using the error signals as inputs, and the corresponding control pulse outputs are applied to the PFC stage to regulate the supply voltage. The CSO-generated output serves as the input to the FOPID controller, facilitating the optimization of its gain parameters. A detailed analysis of the experimental results is presented in Section 4.

RESULTS AND DISCUSSION

In this work, a control topology for the AC–DC converter is developed and implemented using the MATLAB/Simulink platform. The proposed scheme integrates the Cat Swarm Optimization algorithm with a Fractional Order PID controller to minimize error and enhance the efficiency of power factor correction (PFC) in a line-coupled single-stage AC–DC converter. The effectiveness of the controller is examined in the PFC stage, where it significantly progresses the presentation of the boost converter. By optimizing the switching operations, the system achieves precise control pulses, leading to improved stability and efficiency. The equivalent circuit model is used to analyze the operating modes of the boost converter, while the enhanced controller action reduces voltage leakage and ensures smooth operation. The optimized gain parameters generated by the supervisor are practical to the boost switch, ensuring stable and optimized system behavior. The implementation parameters and simulation setup are

presented in this section, with results shown in Figure 4(a) and (b). Finally, the presentation of the anticipated technique is associated with existing optimization techniques, such as the Firefly Algorithm (FA) and Cuckoo Search (CS), and a detailed comparison of parameters is provided in Table 1.

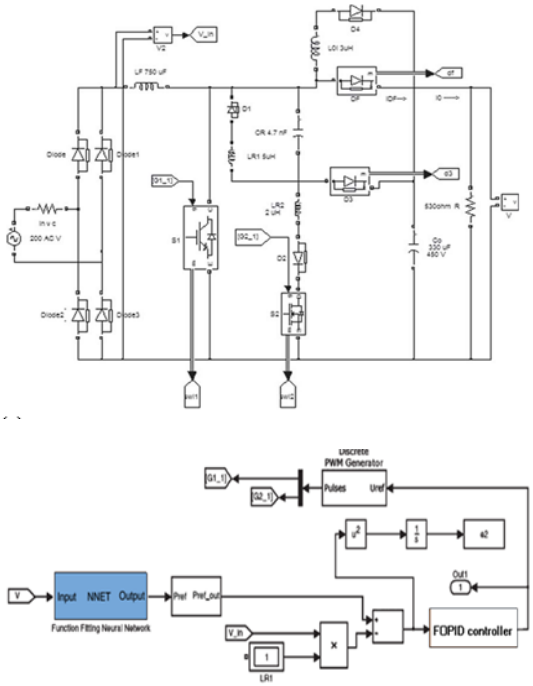


Fig.4 Simulink model, (a) AC to DC converter (b) Proposed controller

Table 1: Implementation parameters of the proposed and existing method

Description	Algorithm	Ranges
No of iterations carried for CSO	CSO	10
No of cats used		02
No of cats seeking mode		01
No of cats tracing mode		01
Population size	CS	50
No of variables		6
No of iterations		10
Lower limits		1
Upper limits		100
Dimension	FA	20
Alpha		0.5
Gamma		1
Lower bound		0.1
Upper bound		10
Beta-min		1

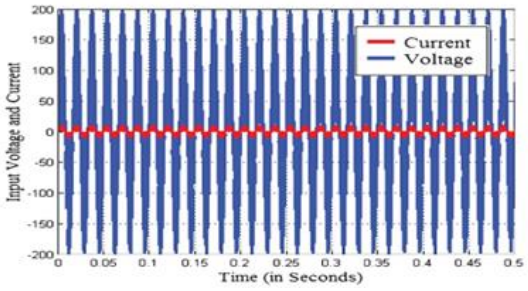


Fig.5 The input voltage and input current waveforms of AC to DC converter

Figure 5 illustrates the input voltage waveform and the corresponding current drawn by the proposed AC–DC converter controlled by the developed algorithm. It is evident that the input voltage and current are nearly in phase, indicating that the converter achieves a near-unity power factor. The X-axis represents time in seconds, while the Y-axis denotes the input voltage and current. From the X-axis, it is observed that the simulation is carried out for a duration of 0.5 seconds.

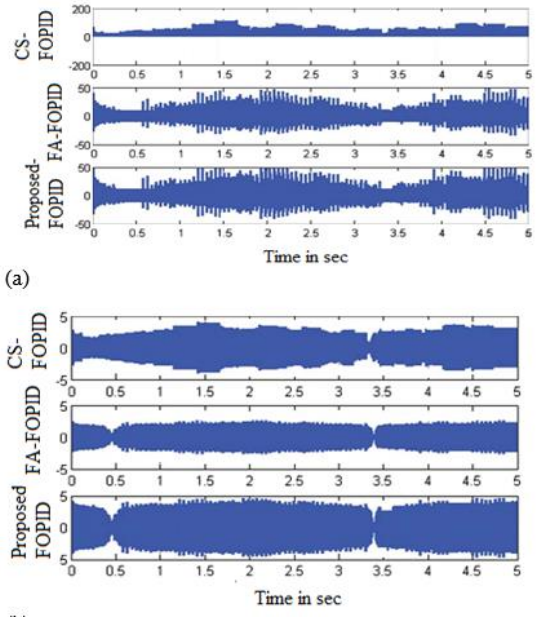


Fig.6: Performance comparison of main inductor (a) voltage and (b) current

The execution of voltage and current waveforms of principle inductor is delineated. Here, the correlation is performed between proposed CSO algorithm, FA, CS calculation based FOPID controller to the converter. From Figure 6 (a) and (b), it says that, for proposed, FA and CS based FOPID controller, the waveforms are having less swells the Proposed CSO based FOPID controller activity.

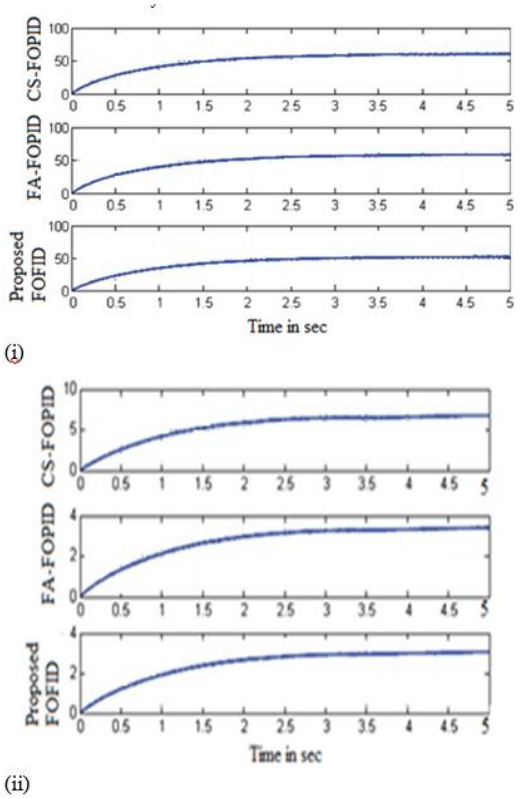


Fig.7 Performance comparison of main switch (a) voltage and (b) current

The voltage and current waveforms of the main switch are illustrated in Figure 7. As shown in Figure 7(i), the voltage waveform obtained using the proposed controller is slightly lower compared to that of the PSO-PID controller and the system without a controller. Meanwhile, Figure 7(ii) depicts the current response of the converter, where the CS-FOPID controller achieves a higher current magnitude compared to both the FA-FOPID and the proposed controller configurations.

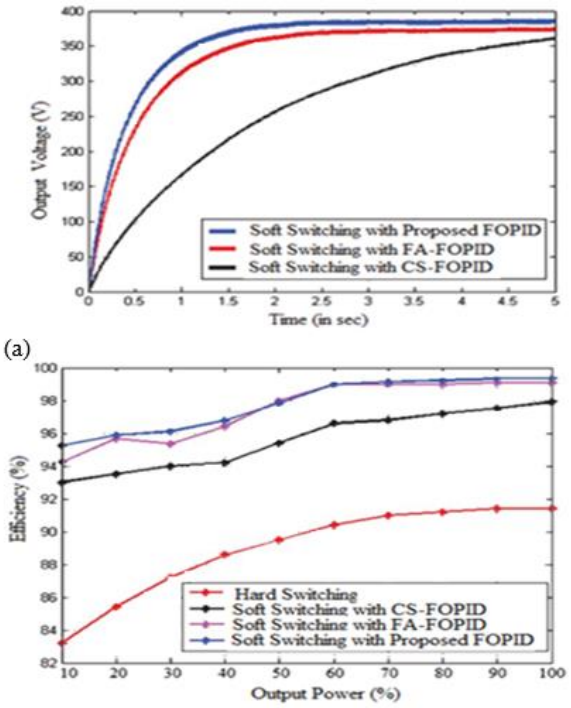


Fig.8 The performance comparison of (a) output DC voltage (b) converter efficiency vs output power

In Figure 8 (a), the execution examination of the novel ideal controller is beautifully shown. It is perfectly clear that, for delicate exchanging without the controller the yield voltage bend has pitiably bombed in landing at the set point and its ascent day and age is high and the settling era likewise far surpasses the replication time frame. Presently, the execution of the effectiveness is surveyed and perfectly imagined in Figure 8 (b). The execution examination of the proposed CSO-FOPID controller with FA-FOPID controller, CS-FOPID controller and hard changing to the AC to DC converter is displayed as far as proficiency versus yield control.

CONCLUSION

This paper presents a Cat Swarm Optimization (CSO) based governor procedure for power factor correction (PFC) in a line-coupled single-stage AC–DC converter. The proposed mechanism strategy aims to achieve optimal converter performance by reducing switching losses and minimizing voltage deviations. By applying optimized PWM switching functions in both boost and PFC operating stages, the method effectively suppresses fault voltages and enhances overall stability. The efficiency of the mechanism performance is validated through implementation in the MATLAB/Simulink environment, where system performance is evaluated in terms of switch voltage and current, inductor voltage, inductance behavior, and overall efficiency. The analysis of the PFC stage demonstrates that the proposed CSO-based approach consistently outperforms conventional methods. Comparative studies with existing algorithms, such as Firefly Algorithm (FA) and Cuckoo Search (CS), further highlight the dominance of the anticipated technique. Simulation results confirm the effectiveness of the CSO procedure in delivering improved dynamic response, reduced error, and enhanced output performance compared to other methodologies.

Conflicts of Interest

The authors declare that there are no conflicts of interest related to the publication of this paper titled "Cat Swarm Intelligence-Driven Optimization for High Power Factor Single-Stage AC–DC Converters." Furthermore, the authors confirm that they have no known competing financial interests or personal relationships that could have influenced the research and findings presented in this work.

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